AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A path searcher for a spread spectrum receiver for receiving a spread spectrum signal containing a scrambled synchronization code, comprising

~~wherein the receiver includes~~ a plurality of correlators, wherein ~~and~~ each correlator produces a replica of said scrambled synchronization code and determines a correlation value between said replica and the received spread spectrum signal,

~~characterized in that~~wherein:

each of said correlators performs a correlation operation between the received spread spectrum signal and said replica at a rate higher than a chip rate of the spread spectrum signal by successively shifting said replica with respect to said spread spectrum signal.

2. (currently amended): The path searcher of claim 1, ~~characterized in that~~wherein each of said correlators comprises:

a multiplier for multiplying said spread spectrum signal and said replica at said higher rate,

an adder for summing an output signal of the multiplier with a previous value, and

a memory for storing an output signal of said adder as an intermediate result of a

correlation value and <u>for</u> supplying the stored signal to said adder as said previous value until the

correlation value is obtained.

    3. (currently amended): A path searcher<u>,</u> for a spread spectrum receiver for receiving a

spread spectrum signal, wherein<u>:</u>

the receiver includes a plurality of correlators, wherein each of the correlators produces a

replica of a scrambled synchronization code and determines a correlation value between said

replica and the received spread spectrum signal<u>,</u> ~~characterized by:~~<u>;</u>

<u>the path searcher comprises:</u> a first memory for storing the received spread spectrum

signal,

~~in that~~ each of said correlators<u>:</u>

    reads the stored spread spectrum signal from the first memory at a rate higher than

a chip rate of said received spread spectrum signal,

    repeatedly performs a correlation operation between the read spread spectrum

signal and said replica at said higher rate by successively shifting said replica with

respect to said stored spread spectrum signal<u>;</u>~~,~~

~~in that there are provided~~<u>the path searcher further comprises</u> a second memory for

initially storing an intermediate result of a correlation value from each of said correlators and <u>for</u>

subsequently reading the stored intermediate result into a corresponding one of said correlators<u>;</u>~~,~~

and

in that each of said correlators adds the intermediate result from the second memory with

a correlation value produced by the correlation operation performed at the end of the chip

interval.

4. (currently amended): The path searcher of claim 3, ~~characterized in that~~wherein each

of said correlators comprises:

a multiplier for multiplying the spread spectrum signal read from the first memory and

said replica at said higher rate,

an adder for summing an output signal of the multiplier with a previous value,

delay means for delaying an output signal of the adder, and

a selector for supplying the delayed output signal to said adder as said previous value

during an initial portion of a chip interval and <u>for</u> supplying the stored intermediate results from

said second memory to said adder at the end of the chip interval.

5. (currently amended): A ~~path searcher for a~~ spread spectrum receiver which receives a

spread spectrum signal containing a scrambled synchronization code, comprising:

a plurality of antenna systems for receiving said spread spectrum signal <u>and</u> for

producing therefrom a plurality of output signals representing characteristics of a plurality of

communication paths;

a plurality of correlators for receiving the output signals of said antenna systems, each

correlator comprising:

a replica generator for producing a replica of said scrambled synchronization code;

a multiplier for performing a multiplying operation between said replica and one of said output signals at a rate higher than a chip rate of said spread spectrum signal by successively shifting said replica with respect to the spread spectrum signal;

an adder for summing an output signal of said multiplier with a previous signal; and

a memory for storing an output signal of said adder and supplying the stored output signal back to said adder as said previous signal.

6. (currently amended): The ~~path searcher~~spread spectrum receiver of claim 5, wherein said multiplier comprises:

a first shift register for storing said replica and recirculating the stored replica along a series of stages;

a second shift register having a plurality of stages divided into a plurality of groups corresponding respectively to stages of a portion of said first shift register,

the stages of each group being connected together to one of the stages of said portion for loading chip data therefrom each time the replica is shifted by one stage in said first shift register and <u>for</u> recirculating the stored chip data along the second shift register; and

a plurality of multiplier units associated respectively with said groups of stages of said

second shift register,

    each of said plurality of multipliers being connected to one of the stages of the

associated group of stages of the second shift register for multiplying one of the output

signals of said antenna systems with the chip data of said second shift register.

7. (currently amended): A ~~path searcher for a~~ spread spectrum receiver which receives a

spread spectrum signal containing a scrambled synchronization code, comprising:

a plurality of antenna systems for receiving said spread spectrum signal and <u>for</u>

producing therefrom a plurality of output signals representing characteristics of a plurality of

communication paths;

a first memory for storing the output signals of said antenna systems for a predetermined

length of chip intervals;

a plurality of correlators for receiving one of the stored output signals from said first

memory, each correlator comprising:

    a replica generator for producing a replica of said scrambled synchronization

code;

    a multiplier for performing a multiplying operation between said replica and the

output signal of said first memory at a rate higher than a chip rate of said spread spectrum

signal while successively shifting said replica with respect to said output signal of said

first memory;

an adder for summing an output signal of said multiplier with a previous signal;

delay means connected to the output of said adder to produce a delayed output signal; and

a selector for initially supplying the delayed output signal repeatedly to said adder as said previous signal to produce an intermediate result of a correlation value at the output of said delay means; and

a second memory connected to the output of the delay means of each of said correlators for storing said intermediate result,

said selector reading the intermediate result from the second memory into said adder to obtain said correlation value when a final result is obtained at the output of said delay means.

8. (currently amended): The ~~path searcher~~ spread spectrum receiver of claim 7, wherein said multiplier comprises:

a first shift register for storing said replica and <u>for</u> recirculating the stored replica along a series of stages;

a second shift register having a plurality of stages divided into a plurality of groups corresponding respectively to stages of a portion of said first shift register, the stages of each group being connected together to one of the stages of said portion for loading chip data therefrom each time the replica is shifted by one stage in said first shift register and <u>for</u> recirculating the loaded chip data along the second shift register; and

a plurality of multiplier units, associated respectively with said groups of stages of said

second shift register, each of said plurality of multiplier units being connected to one of the

stages of the associated group of stages of the second shift register for multiplying a chip stored

therein with one of successively arranged parallel chips of the output signal of said first memory.